Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.067”**

**SOURCE**

**GATE**

**.087”**

**Top Material: Al**

**Backside Material: Cr Ni Ag**

**Bond Pad Size: Gate = .020” X .025”**

**Backside Potential: Drain**

**Mask Ref: GEN 5**

**APPROVED BY: DK DIE SIZE .067” X .087” DATE: 1/17/22**

**MFG: INT’L RECTIFIER THICKNESS .015” P/N: IRFC9024NB**

**DG 10.1.2**

#### Rev B, 7/19/02